(31) VLS2

Reg.No.:								

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 7018

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE 2023
Second Semester
VLSI Design
P19VD206 – LOW POWER VLSI DESIGN
(Regulation 2019)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Realize CMOS logic for 1 bit full adder.	2	K3	CO1
2.	What are the features of sub-micron CMOS Technology?	2	K1	CO1
3.	Write the advantages of Voltage scaling.	2	K1	CO2
4.	Define Velocity saturation.	2	K2	CO2
5.	What is the key to minimize short channel effect?	2	K3	CO3
6.	Differentiate SRAM and DRAM.	2	K2	CO3
7.	Write about the classification of multipliers.	2	K1	CO4
8.	What is the concept of Glitch power dissipation?	2	K1	CO4
9.	Write a list of SPICE commands to estimate gate capacitance.	2	K1	CO5
10.	Draw an AND gate using adiabatic logic.	2	K3	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.			Questions	Marks	KL	CO
11.	a)	i.	Derive an expression for short circuit power dissipation of a CMOS inverter.	9	K3	CO1
		ii.	Write a short note on drain induced barrier lowering.	4	K2	
			(OR)			

	b)	i.	Explain basic principles of low power design.	7	K1	CO1
		ii.	Derive the average dynamic power dissipation for CMOS invertor. Assume the input is V_{in} is a square wave having a period T.	6	K4	
12.	a)	i.	Explain the circuit level techniques for minimization of power dissipation.	8	K3	CO2
		ii.	Explain the concept of state assignment for finite state machine to reduce power dissipation with example.	5	K3	
			(OR)			
	b)		Investigate the characteristics in terms of power dissipation for any two CMOS circuit design styles of full adder circuits.	13	K4	CO2
13.	a)	i.	Differentiate Multi Threshold CMOS (MTCMOS) and Dynamic Threshold Voltage MOS (DTMOS).	5	K1	CO3
		ii.	Explain the working of Dual Cascade Voltage Switch (DCVS) level converter.	8	K3	
			(OR)			
	b)	i.	How the power can be reduced in write driver circuits and sense amplifier circuits?	7	K3	CO3
		ii.	Design a full adder using Adiabatic logic.	6	K4	
14.	a)		Explain in detail about Monte Carlo method for estimating glitch power.	13	K3	CO4
			(OR)			
	b)	i.	Discuss the different methods of estimating average power in combinational circuits.	5	K2	CO4
		ii.	How do you compute signal probability using binary decision diagrams?	8	K3	
15.	a)		Calculate the probabilities and the activities of state inputs using appropriate solution method.	13	K3	CO5
			(OR)			
	b)		Elaborate on the use of pipelining and parallelism for low power.	13	K3	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Discuss the principle of pre-computation logic for reducing power with a suitable example.	15	K3	CO3
		(OR)			
	b)	Explain the techniques used to minimize the software contribution to power dissipation.	15	K3	CO5

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Question Paper Code: 7031

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE 2023
Second Semester
VLSI Design
P19VDE18 – NANO ELECTRONICS
(Regulation 2019)

Time: Three Hours Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	List any two film deposition methods and compare their features.	2	K2	CO1
2.	What is the purpose of chemical mechanical polishing?	2	K2	CO1
3.	How carbon clusters are produced?	2	K2	CO2
4.	What are the properties of carbon nanotubes?	2	K2	CO2
5.	List any two novel materials for logic devices.	2	K1	CO3
6.	What are the advantages of Silicon MOSFETs?	2	K2	CO3
7.	Why high permittivity materials are used for DRAMs?	2	K2	CO4
8.	What is holographic data storage?	2	K1	CO4
9.	List the features of photonic networks.	2	K1	CO5
10.	What are the differences between LED and organic LED?	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Explain any two types of lithography process.	13	K2	CO1
		(OR)			
	b)	Explain the function of any two types of scanning probes.	13	K2	CO1
12.	a)	Explain the fabrication process of carbon nano tubes.	13	K3	CO2
		(OR)			
	b)	Detail any two applications of carbon nano tubes.	13	K3	CO2
13.	a)	Explain the working of ferroelectric field effect transistors.	13	K2	CO3
		(OR)			
	b)	Explain the role of carbon nano tubes in data processing.	13	K3	CO3
14.	a)	Explain the principle of magneto optical disks.	13	K2	CO4
		(OR)			
	b)	Explain the working of rewriteable DVDs based on phase change materials.	13	K2	CO4
15.	a)	Explain the role of nano electronics in data transmission and interfaces.	13	K2	CO5
		(OR)			
	b)	Explain the working of Liquid Crystal Displays.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Comparatively analyze ferro electric random-access memories with magneto- resistive random-access memories.	15	K3	CO4
		(OR)			
	b)	Elaborate the role of nano electronics in microwave communication systems.	15	K2	CO5

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Question Paper Code: 7020

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE 2023
Second Semester
VLSI Design
P19VD207 – TESTING AND VERIFICATION OF VLSI CIRCUITS
(Regulation 2019)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Differentiate testing and verification in VLSI design process.	2	K2	CO1
2.	Define the terms yield and reject rate. Also mention their acceptable values.	2	K1	CO1
3.	Consider the logic circuit F(x) = x1' + x1.x2 = x1' + x2. Compute the set of all tests using Boolean difference method that detect the fault h s-a-1, where h is an input of G1, as shown in Fig. 1.	2	K3	CO2

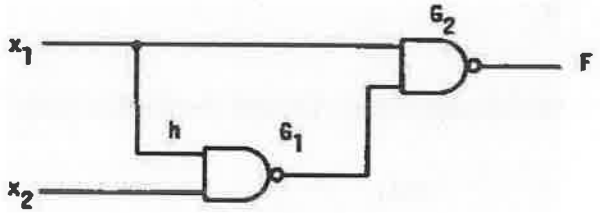

Fig. 1

4.	List the faults that can be detected by IDDQ test.	2	K2	CO2
5.	Suggest a method to detect delay fault in a combinational circuit.	2	K3	CO3
6.	Write short notes on test automation approaches.	2	K2	CO3
7.	At the stage of verification planning, let us assume that you have identified few hard-to-verify features in your design. Which technique can be applied to verify them?	2	K3	CO4
8.	Compare formal and analytical verification approaches.	2	K2	CO4
9.	Specify any two scenarios where logic equivalence checking can be used in the ASIC design flow.	2	K3	CO5
10.	What is static timing analysis?	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Identify the various challenges involved in testing the system on chips and explain.	13	K2	CO1
		(OR)			
	b)	Elaborate the procedure for test generation in VLSI chip fabrication.	13	K2	CO1
12.	a)	Outline the various Ad Hoc Design for Testability techniques and explain how they are different from the algorithmic approaches.	13	K2	CO2
		(OR)			
	b)	Illustrate the boundary scan architecture IEEE 1149.1 and explain how it is used to simplify the testing of a system on a chip.	13	K2	CO2
13.	a)	Highlight the design rules to be followed when designing a logic BIST system.	13	K1	CO3
		(OR)			
	b)	Explain the following memory BIST algorithms and specify their test time complexity and test length. i. March ii. Checkerboard iii. GALPAT iv. Walking 1/0 v. Butterfly	13	K3	CO3
14.	a)	Summarize the various approaches of design verification based on simulation.	13	K2	CO4
		(OR)			
	b)	Model an elevator control for a 3 storey building using verilog constructs and verify the functional correctness with a self-checking testbench.	13	K4	CO4
15.	a)	Describe the role of model checking in the verification of VLSI circuits.	13	K2	CO5
		(OR)			
	b)	Interpret the term hardware emulation and mention how it is different from software emulation.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Consider the circuit shown in Fig. 2 and use PODEM to generate a vector for each of the following faults : i. h s-a-1 ii. f s-a-0	15	K3	CO2

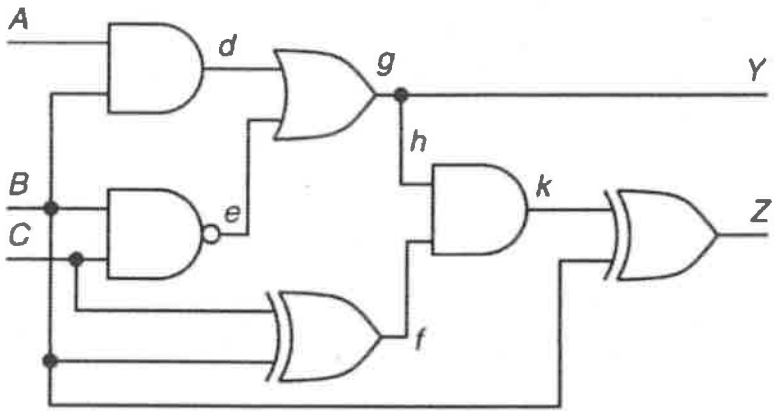

Fig. 2

(OR)

	b)	The circuit in Fig. 3 is the internal layout of a custom built chip. The tpd for each gate is listed below it. The delays for the register are all the same and listed in the lower right corner. Input protection circuits and output fan-out circuitry can slow down the signal transmission on and off the chip. These delays will be represented as simple buffers on the schematic.		K3	CO5
		i. Calculate the worst-case pin-to-pin combinational delay, clock-to-output delay, and register-to register delay.	6		
		ii. Use this data to find the maximum clock frequency.	4		
		iii. Calculate setup and hold adjustments for the external inputs.	5		

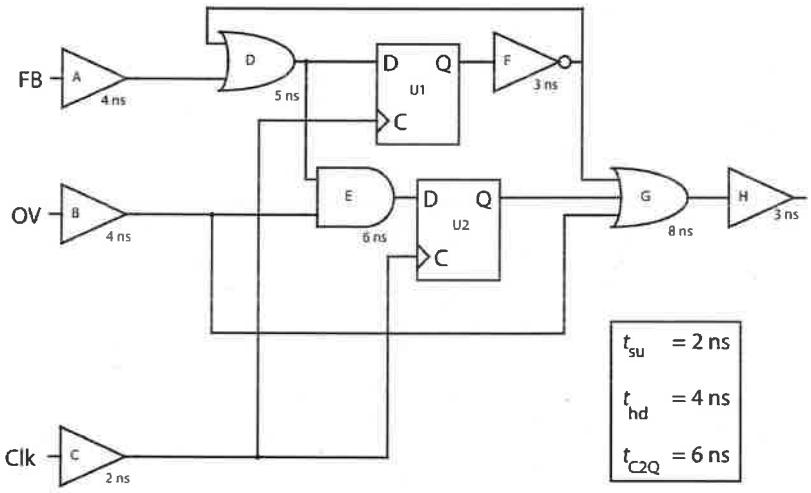

Fig. 3.

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Question Paper Code: 7023

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS –JUNE 2023
Second Semester
VLSI Design
P19VD208 – ASIC DESIGN
(Regulation 2019)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	List the advantages of CMOS Technology.	2	K1	CO1
2.	Compare full custom ASIC & semi custom ASIC.	2	K1	CO1
3.	Write the types of programmable ASICs	2	K2	CO1
4.	Define "PREP" Bench marks.	2	K1	CO3
5.	What are the important file types used in Actel act?	2	K4	CO3
6.	What is the role of logic synthesis in the design flow sequence steps of ASIC?	2	K2	CO1
7.	Compare the types of simulation.	2	K1	CO3
8.	Write the important packages used in VHDL.	2	K1	CO3
9.	Write the objectives of system partitioning.	2	K1	CO5
10.	What is meant by system partitioning?	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.			Questions	Marks	KL	CO
11.	a)	i.	Elaborate on library cell design.	7	K2	CO1
		ii.	Write short notes on Gate array based ASIC.	6	K2	
			(OR)			
	b)		Detail on Data path elements and data path logic cells.	13	K2	CO1

12.	a)	i.	Explain the following: a. EEPROM Technology. b. Antifuse Technology.	3 3	K2	CO2
		ii.	Explain the Actel Act architecture.	7		
			(OR)			
	b)	i.	Elaborate on clock and power inputs.	5	K2	CO2
		ii.	Explain in details about the Xilinx I/O block.	8	K2	
13.	a)	i.	Explain the interconnect architecture used in Xilinx LCA.	8	K2	CO3
		ii.	Give the details of antifuses for Actel ACT family.	5	K2	
			(OR)			
	b)	i.	Write short none on Altera MAX 5000 and 7000.	6	K2	CO3
		ii.	Explain the interconnect architecture used in Altera MAX 5000, 9000.	7		
14.	a)	i.	Write short notes on logic simulation and switch level simulation.	6	K2	CO4
		ii.	Write the different types of modeling used in VHDL & Verilog.	7		
			(OR)			
	b)	i.	Define BIST terminology.	4	K2	CO4
		ii.	Explain serial fault simulation and concurrent fault simulation.	9		
15.	a)	i.	Write the different types of algorithm used in placement.	4	K2	CO5
		ii.	Define floor planning and explain the goals and objectives of floor planning	9		
			(OR)			
	b)	i.	What is meant by circuit extraction and DRC?	4	K2	CO5
		ii.	Write short note on detailed routing and glolal routing.	9		

PART – C

(1 x 15 = 15 Marks)

Q.No.			Questions	Marks	KL	CO
16.	a)	i.	List steps in ASIC physical design and describe goals and objective of each step.	5	K3	CO5
		ii.	Explain the concept of measurement of delay in floor planning.	10		
			(OR)			
	b)	i.	Define "Half gate ASICs" and Define "Schematic entry.	5	K3	CO3
		ii.	Explain the CFI and EDIF connectivity model.	10		

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Question Paper Code: 7026

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE 2023
Second Semester
VLSI Design
P19VDE17 - SYSTEM ON CHIP DESIGN
(Regulation 2019)

Time: Three Hours Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	What are the different types of ASIC? Write their significances?	2	K1	CO1
2.	List the components of embedded SoC.	2	K2	CO1
3.	Enumerate the requirements for SoC design.	2	K3	CO2
4.	What is the differences between soft core on NIOS and hard core?	2	K2	CO2
5.	What is the difference between embedded memory and external memory?	2	K2	CO3
6.	Mention the features of SOC (On-Die) memory systems.	2	K1	CO3
7.	What is functional validation of SoC?	2	K1	CO4
8.	What are the different types of SoC test benches?	2	K1	CO4
9.	Develop a PRSG logic circuit for BIST test.	2	K3	CO5
10.	What is the concept and need of an instruction register of Boundary Scan?	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Enumerate and explain the SoC design issues with examples.	13	K1	CO1

(OR)

	b)	Explain SOC system level interconnection of bus-based approach. Discuss the requirements and specifications in a design process.	13	K2	CO1
12.	a)	How to address the SoC design issues to manage the design complexities? Explain with examples.	13	K3	CO2
		(OR)			
	b)	Write technical notes on 1. On Chip Buses 2. Difference between soft and firm cores.	13	K1	CO2
13.	a)	Compare and contrast embedded memory and flash memory. Explain both in detail with examples.	13	K2	CO3
		(OR)			
	b)	Explain the three stages of PLL. Discuss the use of PLL in SoC with neat diagram and an example.	13	K2	CO3
14.	a)	Define and explain with examples. 1. SoC verification 2. SoC validation 3. SoC testing.	13	K1	CO4
		(OR)			
	b)	Elucidate the concept and significance of hardware /software co-verification with examples.	13	K2	CO4
15.	a)	Discuss in detail about different types of scan design method and explain with neat diagram.	13	K1	CO5
		(OR)			
	b)	Give an account on- TAP controller of Boundary Scan Technique.	13	K1	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Describe the concept of Boundary Scan in detail with supporting diagrams.	15	K2	CO5
		(OR)			
	b)	Explain core level validation with an example.	15	K2	CO4